IEEE International Conference on Integrated Circuit Design and Technology

May 28th – May 30th, 2014

Austin, Texas, USA

www.ICICDT.org

Technical Support:

Site Support:

ICICDT 2014
On behalf of the technical program and organizing committees, we welcome you to the 2014 IEEE International Conference on Integrated Circuit Design and Technology (ICICDT) at the Advanced Micro Devices (AMD) Austin Lone Star Campus in Austin, Texas, U.S.A.

Integrated circuit (IC) engineering roles have traditionally been separated along the boundary between design and technology. As IC products advance toward higher performance and energy efficiency while the time to market continues to accelerate, future IC engineers will require a deep understanding of the interdependencies between design and technology to expand the product optimization window. ICICDT is the forum for engineers, researchers, professors, and graduate students to cross the design-technology boundary through interactions with design, technology, and process experts to develop the skills for future IC research and development. The unique workshop style of the conference fosters an environment for exchanging breakthrough ideas and collaborating effectively. A one-day tutorial program for both the beginner and expert precedes two days of technical presentations and workshops. The 2014 ICICDT topics include:

- Advanced transistors, materials, and processing technologies
- Three-dimensional (3D) integration
- Design for manufacturing, test, yield, and reliability
- Process and design techniques for soft errors, plasma-induced damage, and reliability
- Advanced memory devices and circuits
- RF, analog, and mixed signal circuits
- I/O and electrostatic discharge (ESD) protection circuits
- CAD and design optimizations across system, circuit, and device levels
- Low power systems and circuits
- System-on-Chip (SoC) and system-in-package (SiP) design integration
- Power semiconductor technologies and circuits
- Emerging technologies and circuits

ICICDT is thankful for the technical support from the IEEE Central Texas Section (CTS), the IEEE Electron Devices Society (EDS), the Institute of Electronics, Information, and Communication Engineers (IEICE), and the Japan Society of Applied Physics; and for the site support from Advanced Micro Devices, Inc. (AMD).

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2014 ICICDT Venue:
AMD, Austin Lone Star Campus, 7171 Southwest Parkway, Austin, TX 78735, U.S.A.

ICICDT 2014
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Thursday, May 29th, 2014
Registration, Breakfast, & Workshop Preparation................................. 8:00 AM – 8:30 AM
Opening remarks ..................................................................................... 8:30 AM – 8:45 AM
Keynote Presentation ............................................................................... 8:45 AM – 9:30 AM
Session A: Low Power & System-On-Chip Design .................................. 9:30 AM – 10:10 AM
Coffee Break ......................................................................................... 10:10 AM – 10:30 AM
Session B: Advanced Transistors and Materials .................................. 10:30 AM – 11:30 AM
Workshop A & B ..................................................................................... 11:30 PM – 12:30 PM
Lunch ........................................................................................................ 12:30 PM – 2:00 PM
Session C: I/O Circuits and ESD Protection ......................................... 2:00 PM – 2:40 PM
Session D: Emerging Technologies ...................................................... 2:40 PM – 3:00 PM
Coffee Break ......................................................................................... 3:00 PM – 3:30 PM
Session E: Design Methodologies for Memory and Circuit Reliability .... 3:30 PM – 4:20 PM
Workshop C, D & E ................................................................................. 4:20 PM – 5:20 PM
Dinner Reception: Salt Lick BBQ Restaurant at Driftwood ..................... 7:00 PM - 9:00 PM

Friday May 30th, 2014
Breakfast & Workshop Preparation ....................................................... 8:00 AM - 8:25 AM
Keynote Presentation ............................................................................... 8:25 AM – 9:10 AM
Session F: Advanced Memory Devices & Circuits ................................ 9:10 AM – 9:50 AM
Coffee Break ......................................................................................... 9:50 AM – 10:20 AM
Session G: 3D Integration ..................................................................... 10:20 AM – 11:00 AM
Workshop F & G ..................................................................................... 11:00 AM – 12:00 PM
Lunch ........................................................................................................ 12:00 PM – 1:30 PM
Session H: Gate Dielectric/BTI Reliability and Plasma-Induced Damage .... 1:30 PM – 2:20 PM
Session I: CAD & Design Rules for Advanced Technology Nodes ........ 2:20 PM – 3:00 PM
Coffee Break ......................................................................................... 3:00 PM – 3:20 PM
Session J: Analog and High Voltage Circuits ....................................... 3:20 PM – 4:10 PM
Closing Remarks and ICICDT 2015 Announcement ............................... 4:10 PM – 4:20 PM
Workshop H, I & J ................................................................................... 4:20 PM – 5:20 PM
Post Conference Meeting for TPC ......................................................... 6:00 PM – 9:00 PM

ICICDT 2014
Thursday May 29th

08h00 – 08h30: Registration, Breakfast, & Workshop Preparation

08h30: Conference Opening
Keith Bowman, Qualcomm

08h45: Keynote Presentation
Chair:
Dac Pham, Freescale Semiconductor

The POWER8 Processor: Designed for Big Data, Analytics, and Cloud Environments
Josh Friedrich, IBM

Meeting the needs of evolving server workloads requires new system capabilities to handle massive amounts of increasingly unstructured data and computationally intensive analytic algorithms. At the same time, delivering significant performance gains is increasingly difficult. While technology continues to enable performance growth, extracting those gains requires higher levels of innovation, and increasing complexity drives greater resource investments. In the face of these challenges, POWER8™ delivers a data-optimized design suited for analytics, cognitive workloads, and today’s exploding data sizes. The design point results in a 2.5x performance gain over its predecessor, POWER7+™, for many workloads. Every aspect of the design from the 22nm SOI technology features such as embedded DRAM to the high bandwidth system structure is optimized for larger datasets and new server applications. In addition, POWER8 delivers the efficiency demanded by cloud computing models and also represents a first step toward creating an open ecosystem for server innovation. These new directions set by POWER8 will form the base for all future POWER designs.

Joshua Friedrich is a Senior Technical Staff Member and Manager of POWER™ Technology Development in IBM’s Server and Technology Group. In his current role, Josh is responsible for the design of IBM’s future POWER™ processors. He was the circuit design lead for the POWER8 chip and has been part of the POWER development team since POWER4™. On past POWER™ designs, Josh has led multiple design disciplines including power estimation and reduction, hardware characterization, memory subsystem circuit development, and core execution units. Before joining IBM, Josh received his Bachelor of Science in Electrical Engineering from the University of Texas at Austin.

ICICDT 2014
Session A: Low Power & System-On-Chip Design  
Chairs:  
Michael Han, Qualcomm  
Dac Pham, Freescale Semiconductor  

09h30 **Invited:** Mobile CPU Power/Performance Benchmarking and Process Technology Co-Optimization  
Robert Bucki, Todd Bridges, Tao Xue, Idris Mir, Don Le, Tauseef Kazi, Jeffrey Fischer, Shashank Ekbote, Samit Sengupta, and Giri Nallapati  
Qualcomm  

09h40 **Invited:** A Solar-Powered 280mV-to-1.2V Wide-Operating-Range IA-32 Processor  
Sriram Vangal, Shailendra Jain, and Vivek De  
Intel  

09h50 **Predictive Workload Modeling and Voltage Scaling Using Deep Learning**  
Stephen J. Tarsa, Amit P. Kumar, and H. T. Kung  
Harvard University, Intel  

10h00 **Invited:** Dual function heat-spreading and performance of the IBM / Astron DOME 64-bit µServer demonstrator  
Ronald P. Luijten, Andreas Doering, and Stephan Paredes  
IBM  

10h10 – 10h30: Coffee Break  

ICICDT 2014
Session B: Advanced Transistors and Materials

Chairs:
Dong-Won Kim, Samsung
Bich-Yen Nguyen, SOITEC

10h30 Invited: Variability of Planar Ultra-Thin Body and Buried Oxide (UTBB) FDSOI MOSFETs
Jerome Mazurier
CEA LETI/ST Microelectronics

10h40 STI Fill Effect on Poly-Poly Comb IL
Thuy Dao, Todd Roggenbauer, and Jim Colclasure
Freescale Semiconductor

10h50 Metallization of a Polymer Substrate for Microfluidic-Cooled RF Laminates
Stephen Long\(^1\), Andre Adams\(^2\), Mark Dorsey\(^1\), and Greg Huff\(^3\)
\(^1\)U.S. Naval Research Lab, \(^2\)Texas A&M University

11h00 ALD Ta2O5 and Hf-doped Ta2O5 for BEOL compatible MIM
GLOBALFOUNDRIES

11h10 High-Performance Stacked TiO2-ZrO2 and Si-doped ZrO2 Metal-Insulator-Metal Capacitors
Revathy Padmanabhan\(^1\), Navakanta Bhat\(^1\), S. Mohan\(^1\), Yuichiro Morozumi\(^2\), and Sanjeev Kaushal\(^2\)
\(^1\)Indian Institute of Science, \(^2\)Tokyo Electron

11h20 ALD ZrO2 Processes for BEOL Device Applications
Wenke Weinreich\(^1\), Konrad Seidel\(^1\), Patrick Polakowski\(^1\), Stefan Riedel\(^1\), Lutz Wilde\(^1\), Dina H. Triyoso\(^2\), and Mark G. Nolan\(^2\)
\(^1\)Fraunhofer-Center Nanoelectronic Technologies, \(^2\)GLOBALFOUNDRIES

11h30 Workshop A and B

12h30

12h30 – 14h00: Lunch
**Session C: I/O Circuits and ESD Protection**
Chair:
Philippe Galy, ST Microelectronics

14h00 Invited: RC Triggered Active ESD Clamps; How Should They Behave Under Powered Conditions?
James Miller
Freescale Semiconductor

14h10 New Modular Bi-Directional Power-Switch and Self ESD Protected in 28nm UTBB FDSOI Advanced CMOS Technology
Philippe Galy, Johan Bourgeat, and David Marin-Cudraz
ST Microelectronics

14h20 Pull-Up/Pull-Down Line Impedance Matching Methodology for High Speed Transmitters
Armen Durgaryan¹, Abraham Balabanyan¹, Vazgen Melikyan¹, and Khaldoon Abugharbieh²
¹Synopsys, ²Princess Sumaya University for Technology

14h30 32% Slew Rate and 27% Data Rate Improved 2xVDD Output Buffer Using PVTL Compensation
Tzung-Je Lee¹, Kai-Wei Ruan², and Chua-Chin Wang²
¹Cheng Shiu University, ²National Sun Yat-Sen University

**Session D: Emerging Technologies**
Chairs:
Simon Deleonibus, LETI
Hiroshi Mizuta, University of Southampton

14h40 Invited: Bio-Integrated Electronics
Nanshu Lu
University of Texas at Austin

14h50 Invited: Emerging Research Device Roadmap and Perspectives
An Chen
GLOBALFOUNDRIES

15h00 – 15h30: Coffee Break
Session E: Design Methodologies for Memory and Circuit Reliability
Chairs:
Rouwaida Kanj, American University of Beirut
Minsik Cho, IBM

15h30 Invited: Robust Low-Power Reconfigurable Computing with a Variation-Aware Preferential Design
Saibal Mukhopadhyay¹ and Swarup Bhunia²
¹Georgia Institute of Technology, ²Case Western

15h40 Invited: Modeling SRAM Dynamic Vmin
Ben Calhoun
University of Virginia

15h50 Robust Bias Temperature Instability Refresh Design and Methodology for Memory Cell Recovery
Gerard Touma¹, Rouwaida Kanj¹, Rajiv Joshi², Ayman Kayssi¹, and Ali Chehab¹
¹American University of Beirut, ²IBM

16h00 Testing, Diagnosis and Repair Methods for NBTI-Induced SRAM Faults
Bao Liu and Chiung-Hung Chen
University of Texas at San Antonio

16h10 Cross Logic: A New Approach for Defect-Tolerant Circuits
Mariem Slimani, Arwa Ben Dhia, and Lirida Naviner
Institut TELECOM

16h20 Workshop C, D, and E

17h20

19h00 – 21h00: Dinner Reception
Salt Lick BBQ Restaurant at Driftwood
08h00 – 08h25: Breakfast & Workshop Preparation

08h25: Keynote Presentation
Chair:
Bich-Yen Nguyen, Soitec

Innovation Pipeline for 10nm and beyond

Mukesh Khare, IBM

Dr. Mukesh V. Khare is an IBM Distinguished Engineer and Director at Albany NanoTech Research Center in New York and is responsible for the semiconductor technology research for sub-10nm node. In his current role, he is leading IBM’s joint development alliance with top semiconductor companies to define next generation technology, generate silicon proof points and develop longer term pipeline of innovative elements. Dr. Khare led the development and implementation of high-k metal gate technology starting from fundamental research to full implementation in 32nm technology node at IBM and development alliance member companies. He and his research team drove the development of three dimensional device structure called FinFET that delivers superior power performance benefit to IBM and its development alliance partners. The FinFET innovation under his leadership is being implemented at IBM’s 300mm Fishkill Fab for qualification and volume production. As a technical champion, he led engineering team through development and qualification of the 90nm SOI technology from basic definition to the transfer in manufacturing Fab. Dr. Khare is a recipient of Corporate Award and Outstanding Technical Achievement Award at IBM towards his technical contribution and leadership. He is an officer and technical program committee member at the Symposia on VLSI Technology. He has authored and co-authored more than 80 research papers and holds several U.S. and international patents. Dr. Khare received his M.S., M. Phil., and Ph.D. degrees in Electrical Engineering from Yale University and has been working at various engineering and executive positions at IBM since 1998.
Session F: Advanced Memory Devices & Circuits
Chairs:
Mark Hall, Freescale Semiconductor
Hideto Hidaka, Renesas

09h10 **Invited:** FinFET SRAM Design Challenges
David Burnett
GLOBALFOUNDRIES

09h20 Single-Ended Sub-Threshold FinFET 7T SRAM Cell Without Boosted Supply
Chandrabhan Kushwah, S. K. Vishvakarma, and D. Dwivedi
IIT Indore

09h30 **Invited:** Highly-Reliable TaOx ReRAM Technology using Automatic Forming Circuit
Akifumi Kawahara and Ken Kawai
Panasonic

09h40 A Sub-Threshold Eight Transistor (8T) SRAM Cell Design for Stability Improvement
Chandrabhan Kushwah, S. K. Vishvakarma, and D. Dwivedi
IIT Indore

09h50 – 10h20: Coffee Break

Session G: 3D Integration
Chairs:
Dina Triyoso, GLOBALFOUNDRIES
Bich-Yen Nguyen, SOITEC

10h20 **Invited:** Pathfinder3D: A Framework for Exploring Early Thermal Tradeoffs in 3DIC
Shivam Priyadarshi, Rhett Davis, and Paul Franzon
North Carolina State University

10h30 3D Serial TSV Link for Low-Power Chip-to-Chip Communication
Giulia Beanato, Alessandro Cevrero, Giovanni De Micheli, and Yusuf Leblebici
EPFL

10h40 A Comparative Analysis of 3D-IC Partitioning Schemes for Asynchronous Circuits
Landon Caley, Chien-Wei Lo, Francis Sabado, and Jia Di
University of Arkansas

10h50 Thermal-Driven 3D Floorplanning using Localized TSV Placement
Puskar Budhathoki, Andreas Henschel, and Ibrahim (Abe) M. Elfadel
Masdar Institute of Science and Technology

ICICDT 2014
11h00  Workshop F and G
12h00  

12h00 – 13h30: Lunch

Session H: Gate Dielectric/BTI Reliability and Plasma-Induced Damage
Chairs:
Yuichiro Mitani, Toshiba Corporation
Koji Eriguchi, Kyoto University

13h30  Invited: Assessing Device Reliability through Atomic-Level Modeling of Material Characteristics
Gennadi Bersuker
SEMATECH

13h40  Invited: Characterization and Modeling of Charge Trapping: from Single Defects to Devices
Tibor Grasser¹, Gerhard Rzepa¹, Michael Walt¹, Wolfgang Goes¹, Karina Rott², Hans Reisinger², and Ben Kaczer²
¹TU Wein, ²Infineon, ³IMEC

13h50  Understanding Timing Impact of BTI/RTN with Massively Threaded Atomistic Transient Simulations
Dimitrios Rodopoulos¹, Dimitrios Stamoulis¹, Grigorios Lyras¹, Dimitrios Soudris¹, and Francky Catthoor²
¹National Technical University of Athens, ²IMEC & KU Leuven

14h00  Random Telegraph Noise as a New Measure of Plasma-Induced Charging Damage in MOSFETs
Masayuki Kamei, Yoshinori Takao, Koji Eriguchi, and Kouichi Ono
Kyoto University

14h10  A New Aspect of Plasma-Induced Physical Damage in Three-Dimensional Scaled Structures
Koji Eriguchi, Yoshinori Takao, and Kouichi Ono
Kyoto University

ICICDT 2014
Session I: CAD & Design Rules for Advanced Technology Nodes
Chairs:
Rouwaida Kanj, American University of Beirut
Minsik Cho, IBM

14h20 Invited: A Review on Contemporary High Level Synthesis
Haoxing Ren
IBM

14h30 Efficient Computation of Combinational Circuits Reliability Based on Probabilistic Transfer Matrix
Lirida Naviner, Kaikai Liu, Hao Cai, and Jean-Francois Naviner
Institut Mines-TELECOM

14h40 A High-Level Design Rule Library Addressing CMOS and Heterogeneous Technologies
Gérald Cibrario, Marjorie Gary, Fabien Gays, Karim Azizi-Mourier, Olivier Billoint, Ogun Turkyilmaz, and Olivier Rozeau
CEA-LETI

14h50 Design Layout Optimization in the Presence of Proximity-Dependent Stress Effects
Akif Sultan¹,², M. Rashad Ramzan¹, and Derick Wristers²
¹United Arab Emirates University, ²GLOBALFOUNDRIES

15h00 – 15h20: Coffee Break

Session J: Analog and High Voltage Circuits
Chair:
Thuy Dao, Freescale Semiconductor

15h20 Invited: Piezoelectric Soft MEMS for Tactile Sensing and Energy Harvesting
F. Guido, V. Mastronardi, S. Petroni, and M. De Vittorio
Istituto Italiano di Tecnologia

15h30 A 10 Gbps Loss of Signal Detector for High-Speed AC-Coupled Serial Transceivers in 28nm CMOS Technology
Sanad Kawar, Khaldoon Abugharbieh, Waseem Al-Akel, and Mahmood Mohammed
Princess Sumaya University for Technology

15h40 A Low-Jitter Clock and Data Recovery for GDDR5 Interface Trainings
Yuan Fang, Jonas Bargon, Ashok Jaiswal, and Klaus Hofmann
TU Darmstadt

15h50 Design of a Voltage Reference Circuit Based on Subthreshold and Triode MOSFETs in 90nm CMOS
Mahmood Mohammed, Khaldoon Abugharbieh, Mahmoud Abdelfattah, and Sanad Kawar
Princess Sumaya University for Technology

ICICDT 2014
16h00  An On-Chip High-Voltage Current Sensor for Battery Module Monitoring
Chua-Chin Wang, Wen-Je Lu, and Sheng-Syong Wang
National Sun Yat-Sen University

16h10  Closing Remarks

16h15  2015 ICICDT Announcement

16h20  Workshop H, I and J

17h20